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A Review on High Speed CMOS Counter Using Altera MAX300A

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Abstract: Counters are widely used as essential building blocks for a variety of circuit operation. This paper present a high-speed wide-range parallel counter that achieves high operating frequencies through a state look-ahead methodology .It is a synchronous counter in which all modules are triggered at the same clock edge. The state look-ahead path prepares the counting path's next counter state prior to the clock edge such that the clock edge triggers all modules simultaneously, thus propagation delay is avoided. The advantages for this counter is using only three module types it can be expanded to N-bit counter. Secondly there is no fan-in or fan-out increase. And the propagation delay can be minimized thus operating frequency can be improved.

Keywords: Counting path, state look – ahead logic, operating frequency, chip area**.**

I. INTRODUCTION

A digital counter is a set of flipflops whose states change in response to pulses applied at the input to the counter. Counters are widely used as essential building blocks for a variety of circuit operations , such as code generators ,programmable frequency dividers, shifters, memory select management, and various arithmetic operations. Since many applications are comprised of these fundamental operations, much research focuses on efficient counter architecture design. Counter architecture design methodologies explore tradeoffs between amount of power consumption , operating frequency, size of the device, and target application specialization.

In the previous design , the counter operating frequency was improved by partitioning large counters into multiple smaller modules, such that modules of higher significance were enabled when all bits in all modules of lower significance saturate. Subsequent methodologies improved counter operating frequency using half adders in the parallel counting modules .The maximum operating frequency was limited by the half adder module delay, DFF access time, and the detector logic delay.

In this design modifications are enhanced AND gate delay, and subsequently operating frequency, by redistributing the AND gates to a smaller fan-in and fan-out layout separated by latches. However, the drawback of this redistribution was increased count latency. In addition, this counter architecture inherited an irregular VLSI layout structure and resulted in a large area overhead**.**

II. REVIEW OF EXISTING SYSTEM

It is a carry select counter that have high counting and sampling rates and low cost at the same time. Fig.1 presents a 12-bit carry-select counter. The counter is composed of three sections with 1, 2, and 9 bits respectively, starting with the least significant bit for the count. If the number of bits required is smaller than 12, remove flip-flops, and the associated Half Adders and AND gates, that are not needed. Each of the sections includes an incrementer, which act as a carry-ripple adder with addend 1, the same as a carry-ripple counter with input 1 or a carry-anticipate counter .The enable signal of each section is the logical AND of carry-out signals from all the previous sections. The minimum counting period of carry-select counters is the delay of a 3-input AND gate plus the time required for loading a flip-flop. A 12-bit carry-select counter is shown.

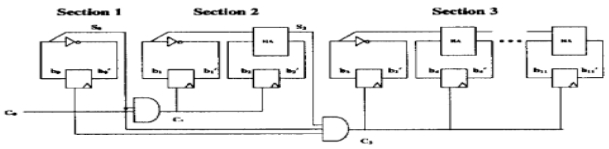

Fig 1. 12-bit carry-select counter

But the drawbacks of this system is its irregular structure and power consumption is very high.

For various arithmetic operations several modern counter designs are well suited, such as systolic counters and population counters. Systolic counters have high operating frequencies at the expense of representing the count value using two redundant binary numbers, which results in a large area overhead for state decoding. Population counters and counting responders provide high operating frequencies using the relationship between counter inputs and outputs based on listing all input bits. Finally, these alternative counter designs increase counter operating frequency using ratioed logic dynamic DFFs , but however these designs tended to have large area overheads making them not ideal for continued CMOS technology scaling.

III.EXPERIMENTAL SETUP

The block diagram of CMOS parallel counter System is

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shown in figure 2. It consists of Counting path (controls counting operation) and State look-ahead path (anticipates future states and thus prepares the counting path for these future states).

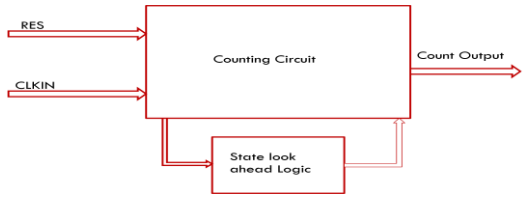

Figure 2 .Block Diagram representation

The state look-ahead path bridges the anticipated overflow states to the counting modules, which are exploited in the counting path. The counting modules are partitioned into smaller 2-bit counting modules separated by pipelined DFF latches.

Subsequently, all counting states and all pipelined DFFs are triggered concurrently on the clock edge, enabling the count state in modules of higher significance to be anticipated by the count state in modules of lower significance. This cooperation between the counting path and state look-ahead paths enables every counting module (both low and high significance) to be triggered concurrently on the clock edge without any rippling effect.

IV.PARALLEL COUNTER ARCHITECTURE

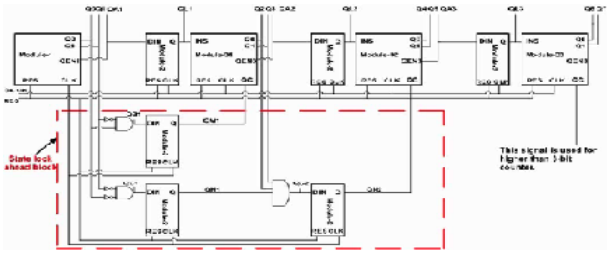

Figure .3

Fig. 3 depicts the proposed parallel counter architecture for an 8-bit counter. The main structure consists of the state look-ahead path (all logic encompassed by the dashed box) and the counting path (all logic not encompassed by the dashed box).

The counter is constructed as a single mode counter, which sequences through a fixed set of preassigned count states, of which each next count state represents the next counter value in sequence. The counter is partitioned into uniform 2-bit synchronous up counting modules. Next state transitions of higher significance are enabled on the clock cycle preceding the state transition using stimulus from the state look- ahead path. Therefore, all counting modules concurrently transition to their next states at the rising clock edge (CLKIN).

V.ARCHITECTURAL FUNCTIONALITY

The counting path's counting logic controls counting operations and the state look-ahead path's state look-ahead logic anticipates future states and thus prepares the counting path for these future states. Fig. 3 shows the three module types (module-1, module-2, and module-3S, where S=1, 2, 3, etc. (increasing from left to right) and represents the position of module-3) used to construct both paths. Module and module-3 are exclusive to the counting path and each module represents two counter bits.

I. Module-2 is a conventional positive edge triggered DFF and is present in both paths. In the counting path, each module-3 is preceded by an associated module-2. Module- 3's serve two main purposes. Their first purpose is to generate all counter bits associated with their ordered position and the second purpose is to enable future states in subsequent Module-3 S's in conjunction with stimulus from the state look ahead path.

VI.HARDWARE IMPLEMENTATION

HARDWARE DESCRIPTION OF MODULE -1

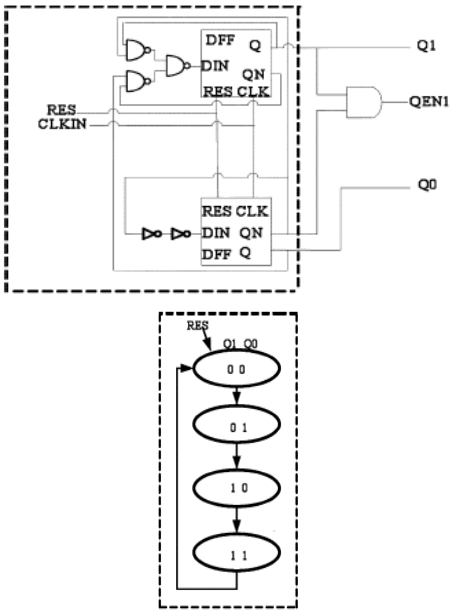

Figure 4 -State diagram of Module-1

Module-1 is a standard parallel synchronous binary 2-bit counter, which is responsible for low-order bit counting and generating future states for all module-3 's in the counting path by pipelining the enable for these future states through the state look-ahead path. Fig. 4. depicts the (1) hardware schematic and (2) state diagram for module-1. Module-1 outputs Q1Q0 (the counter's two low-order bits) and QEN1=Q1 ANDQ¯0. QEN1connects to the module-2's DIN input.

The placement of module-2s in the counting path is critical to the novelty of the counter structure. Module-2s in the counting path act as a pipeline between the module-1 and module-3 1 and between subsequent module 3-S.Module - 2 placements increases counter operating frequency by eliminating the lengthy AND-gate rippling and large AND gate fan-in and fan-out typically present in large width parallel counters.

Thus, instead of the modules of higher significance requiring the ANDing of all enable signals from modules of lower significance, modules of higher significance (module-3S) are simply enabled by the module3-S,s preceding module-2 and state look ahead logic.

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Since the coupling of module-2 with module an extra cycle delay before module-3 1 is enabled, module-2's DIN is triggered when the module-1's count Q1Q0=10

Thus, the module-2s in the counting path provide a 1-cycle look-ahead mechanism for triggering the module-3S's , enabling the module-2s to maintain a constant delay for all stages and all module-3 's to count in parallel at the rising clock edge instead of waiting for the overflow rippling in a standard ripple counter.

HARDWARE DESCRIPTION OF MODULE -3

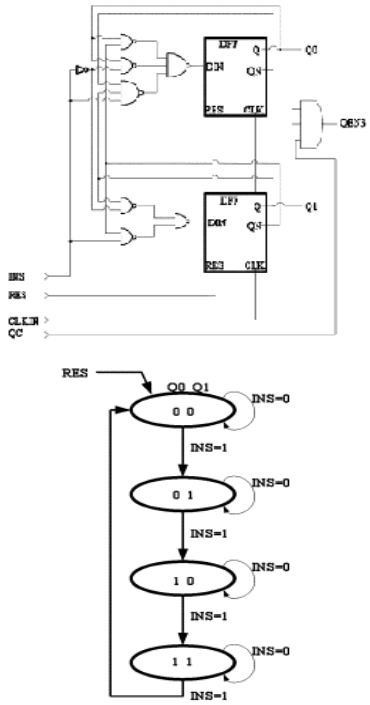

Figure 5-State diagram of Module-3

Fig. 5 depicts the (1) hardware schematic and (2) state diagramfor module-3 . Module-3 is a parallel synchronous binary 2-bit counter whose count is enabled by INS . INS connects to the Q output of the preceding module-2. Module-3S outputs Q1Q0 (which connect to the appropriate count output bits QX and Q(X-1) as shown in Fig. 1) and QEN3=Q1AND Q0 AND QC (the 3 in QEN3 denotes that this is the QEN for module-3S). The state look-ahead logic provides the QC input. QEN3 connects to the subsequent module-2's DIN input and provides the one-cycle look ahead mechanism.

VII. STATE LOOK –AHEAD PATH

The state look-ahead path operates similarly to a carry look-ahead adder in that it decodes the low-order count states and carries this decoding over several clock cycles in order to trigger high-order count states. The state look-ahead logic is principally equivalent to the one-cycle look-ahead mechanism in the counting path. For example, in a 4-bit counter constructed of two 2-bit counting modules, the counting path's module-2 decodes the low-order state Q1Q0=10 and carries this decoding across one clock cycle and enables Q3Q2=01 at module-3 1 on the next rising clock edge. This operation is equivalent to decoding Q1Q0=11 and enabling on the next immediate rising clock edge. The state look-ahead logic expands this principle to an X -cycle look-ahead mechanism. This state look-ahead logic organization and operation avoids the use of an overhead delay detector circuit that decodes the low order modules to generate the enable signals for higher order modules, and enables all modules to be triggered concurrently on the clock edge, thus avoiding rippling and long frequency delay.

Generalized N-bit counter

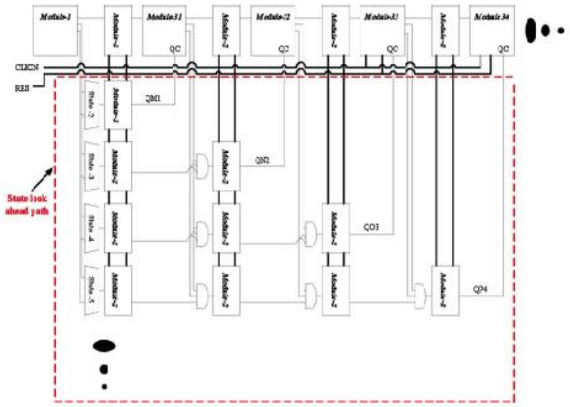

Fig. 6 N -bit counter

The generalized N -bit counter topology, revealing state look-ahead path details. Module-2s in the state look-ahead logic are responsible for propagating (pipelining) the early overflow detection to the appropriate module-3S. Early overflow is initiated by the module-1 through the left-most column of decoders (state-2, state-3, etc.). The Q output of the right-most module-2 (QM1, QN2 etc.) in each early overflow pipelining chain is connected to the input of the appropriate module-3S. The module-3S 's output QEN3=Q1 AND Q0 AND QC , signaling that not only has that module-3S overflowed, but all modules preceding that module-3 have also overflowed, thus enabling the count in the subsequent module-3(S+1) .

Each State- block consists of simple two-input AND logic that decodes the module-1's Q1Q0 output. Fig. 2.2 shows the internal logic for *State-2* and *State-3* as$\bar{Q}$1Q0 and Q1Q0 respectively, and whose outputs QB1and QC1 (as in Fig. 2), respectively, are connected to the appropriate module-2s DIN input, thus starting the early overflow pipelining exactly X clock cycles before the overflow must be detected to enable counting in a module-3S . It is noted that module-1 and module-3S may be of arbitrary bit width, and thus the same look-ahead principle would equally apply.

VIII .MODIFIED SYSTEM

EXTENDED SEQUENTIAL LOGIC

In the modified circuit extended sequential logic is used. The extension of sequential logic functionality of D flip-flop in order to perform an additional Boolean function simultaneously along with its usual bit-storage function. It is shown that a combinational function of the form ($a \cdot b$), ($a + b$), ($a + \bar{b}$), or ($\bar{a} \cdot b$) which occurs frequently in a feed forward path with a *D* flip-flop could be

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implemented efficient sequential logic is found to result in a significant reduction in critical path and saving in area complexity over the direct implementation. In this system all gates are replaced by D flip-flop, so that the total area can be saved effectively. The combinational logic in feed forward path with a sequential element like a *D* flip-flop serves usually the same function when combinational function precedes the sequential one and vice versa.

The replacement of AND gate with D flip flop is shown below. NS and NC stand for "next state" and "no change," respectively.

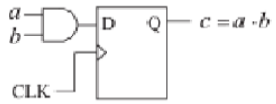

Figure 7 Logic symbol of AND followed by *D* flip-flop

clock	a	B	N.S
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1
0	x	X	N.C

Figure8- State-transition table

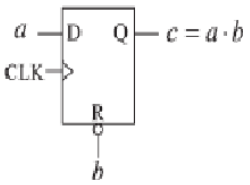

Figure 9 -Extended sequential logic implementation of an AND gate followed by a *D* flip-flop.

The logic symbol of an AND operation (c = a · b), and subsequent storage of output bit c by a D flip-flop, is shown in Fig.7. A combination of truth table of AND gate and state-transition table of a positive edge triggered D flip-flop is shown as state-transition-truth table in Fig. 8. The same function as that of AND gate followed by D flip-flop can be obtained by using a as D input and b as active-low synchronous RESET of a D flip-flop, as shown in Fig. 9. It is easy to find that the arrangement of Fig. 9 has the same truth table as that in Fig. 8. Similarly all gates were replaced by D Flip Flop, so that the total area can be saved effectively.

IX.SOFTWARE IMPLEMENTATION

The synthesis and simulation results for the 8-bit parallel counter is done. Here the functional verification is provided using a synthesized HDL representation using the software MODELSIM 6.3f. Simulation waveforms for a synthesized HDL representation of 8-bit parallel counter operating on an Altera MAX300A device is shown in fig 10. The area and power consumption can be calculated using the simulation software called Xilinx ISE 8.1i . .

X. EXPERIMENTAL RESULTS

Simulation waveforms for a synthesized HDL representation of 8-bit parallel counter operating on an Altera MAX300A device is shown in fig 10. The clock (SCLK) frequency is 250 MHz and $V_{dd=}$4 V.

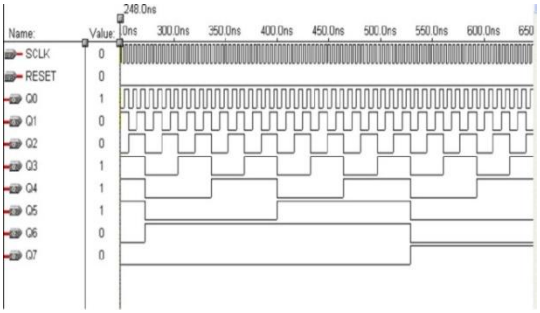

Figure 10 -Simulation waveform

XI .COMPARISON RESULTS

Table shows the comparison results of our parallel counter to counter designs by Alioto, Kakarountas and Yeh in terms of power consumption in milliwatts, maximum clock frequency in gigahertz, and area requirements in number of transistors for an 8-bit counter.

Alioto et al	*Technology (µm/VDD)*	*Power consumption (mW)*	*Speed (GHz)*	*Area (no.of transistors)*	*Design drawbacks*
Alioto et al	*0.18/1.8V*	*221*	*0.5*	*160*	*Requires biasing circuits*
yeh et al	*0.15/1.5V*	*7.64*	*1.1*	*373*	*Irregular structure & outpui lateny*
Kakarountas et al	*0.6/5V*	*21.3*	*0.467*	*286*	*Irregular structure & o/p not in binary*
parallel counter	*0.15/1.5V*	*13.89*	*2*	*510*	*large area*

XII . CONCLUSION

In this paper, a high-speed CMOS counter is presented. The state look-ahead path logic and pipelined paradigm are the main features of this counter. Due to this all modules are activated concurrently at the system's clock edge, thus providing all counter outputs at the exact same time ,thus avoids ripples.

In addition, this structure uses a VLSI scaling technology, which is forming a pattern paradigm. There is no increase in fan-in or fan-out as the counter width increases, resulting in a uniform frequency delay that is attractive for parallel designs. Using advanced circuit design techniques the counter frequency is improved. In order to avoid setup and hold time violations extra precautions must be considered during synthesis or layout implementations.

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